

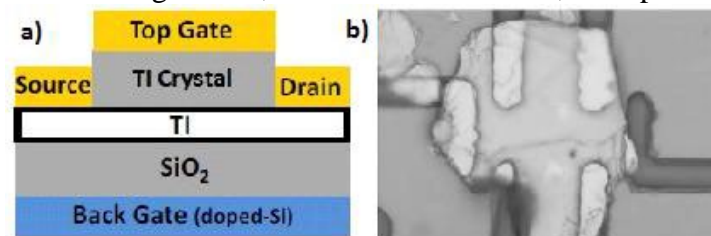
# Investigating topological insulators towards spintronics devices

James Porter, Vahid Tayari, A. R. Champagne

**Keywords:** Topological Insulators, nanoelectronics, nanotechnology, spintronics, Quantum Hall Effect

## **Background and Significance**

Topological Insulators (TIs), a recently discovered family of crystals [1,2], have the interesting property that their bulk acts as an insulator due to an energy gap between their valence and conduction bands, whereas their surfaces (or edges, if 2D), can support a current which is spin-polarized. The surface states travel in opposite directions depending on their spin, and these states are resistant to scattering. Adding a gate to very thin TI devices allows for tuning the energy spectrum in and out of the spin polarized regime (potential spintronics devices). We will explore this phenomenon, and TI correlated electronic states such as room temperature dissipation-free edge states, excitonic condensates, and spin transistors.



**Fig 1:** (a) Model of a double gated TI device on Si/SiO<sub>2</sub> substrate.  
 (b) Six photolithographically defined electrodes on a Bi<sub>2</sub>Se<sub>3</sub> crystal

## **Methodology**

Using Si/SiO<sub>2</sub> wafers as our substrate, we use reactive ion etching (RIE) to etch the backside SiO<sub>2</sub> to allow for back-gate connection. We then carry out photolithography on the SiO<sub>2</sub> surface to define a grid, which we use to locate flakes. We use bulk crystals of Bi<sub>2</sub>Se<sub>3</sub> to synthesize few nm-thick 3D TI nanoflakes. We deposit flakes on our substrates at Concordia either by mechanical exfoliation of bulk crystals (scotch tape), or growth by chemical vapor deposition (we use a powdered bulk sample). We then characterize them by optical microscopy and AFM. The Bi<sub>2</sub>Se<sub>3</sub> forms quintuple layers of atomic planes, and the number of atomic layers is determined from the thickness of the flake. After finding a suitable flake, we place electrodes by photolithography (Fig 1b). After the electrodes have been defined, they are metallized by electron beam evaporation. We then wire bond the chip to a carrier. We will build devices which are back-gated, as well as double-gated ones (Fig. 1a) to allow the tuning of the energy spectrum (in and out of the spin-polarized regime). Our lab is equipped to make precise electron transport measurements at temperatures ranging from 0.3K - 420K, and in magnetic fields of up to 14T. Over this range we will probe this new class of materials to learn about dissipation free edge states, excitonic condensates, and the potential of topological insulators for spin transistors.

**Collaborators:** Roger Müller, Andrea Bianchi (Université de Montréal)

## **References:**

[1] Xiao-Liang Qi, Shou-Cheng Zhang, *Topological insulators and superconductors*;  
[http://arxiv.org/PS\\_cache/arxiv/pdf/1008/1008.2026v1.pdf](http://arxiv.org/PS_cache/arxiv/pdf/1008/1008.2026v1.pdf).

[2] Liang X. and Zhang S.C (2010, January), *The quantum spin Hall effect and topological insulators*. Physics Today, 33-38.

**Funding:** NSERC, Concordia, CFI